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09/905,786	07/13/2001	Christian Willibald Bohm	APD1529	4008

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Matthew E. Connors
Samuels, Gauthier & Stevens, LLP
Suite 3300
225 Franklin Street
Boston, MA 02110

EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,786	BOHM ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 28, 2005 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 17-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 22 and 28 are rejected under 35 U.S.C. 102(e) as being anticipate by Hebbalalu et al (US Patent No. 6,130,719).

In considering claim 22, Hebbalalu et al discloses all claimed subject matter, note 1) the claimed determining time-varying properties of the input signal having the

synchronization pulse is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), and 2) the claimed detecting, from said predetermined, time-varying properties of the input signal the presence of the synchronization pulse is met by the digital circuit 230 which includes the pulse type detection circuit 620 receives the output of operational amplifier 250 and determines whether a valid pulse is present (Fig. 6, col. 5, line 58 to col. 7, line 12).

In considering claim 28, Hebbalalu et al. discloses all the claimed subject matter, note 1) the claimed an detector responsive to samples of the input signal for separating substantially an non-time varying portion of the input signal from a substantially time varying portion of the input signal is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), 2) the claimed a timer for determining the time duration of one of the portions, and the claimed a processor for detecting the synchronization pulse in response to the determined time duration is met by the control circuit which measures the length of duration in terms of number of clock ticks and set boundary register 610 which control the operation of the clamp state machine 650, for example, the maximum and minimum number of clock

ticks representing the duration of a valid HSYNC pulse (Fig. 6, col. 5, line 58 to col. 7, line 12).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 17-20, 23-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebbalalu et al. (US Patent No. 6,130,719) in view of Hulvey (US Patent No. 5,844,622).

In considering claim 17, Hebbalalu et al discloses all claimed subject matter, note the claimed a shape detector for processing samples of an input signal having a synchronization pulse and a plurality of non-synchronization pluses to determine whether such samples have a predetermined sequence; said predetermined sequence

being a first, non-time varying portion, followed by a first, time-varying portion, followed by a second, non-time varying portion, followed by a second, time varying portion followed by a third, non-time varying portion, one of the first and second, time varying portion having a positive slope and the other one of the first and second, time varying portion having a negative slope is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56).

However, Hebbalalu et al explicitly do not disclose the newly added limitation wherein the slope of the time varying portions are determined by comparing said input signal to a specified criterion based in part of the various slop requirements for the time varying portions.

Hulvey teaches that the falling edge detector 86 essentially forms a circuit with looks for a point in the digitized video signal 14 where the cumulative drop in the three samples is greater than or equal to eight (8) and the last value was less than or equal to two (2), when this condition occurs, the falling edge of the digitized horizontal sync pulse 16 has been detected, the outputs from the binary weighted comparators 102 and 106 are each applied to an AND gate 108, if both inputs to the AND gate to high indicating a flat portion followed by a steep slope (i.e. falling edge), and the AND gate 108 outputs a high timing pulse identified as the external horizontal sync pulse 30 (Figs. 2A and 2B, col. 5, line 35 to col. 7, line 32).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the slope determination as taught by Hulvey into Hebbalalu et al's system in order to accurately detecting and processing horizontal synchronization pulse in the analog video signal.

In considering claim 18, the claimed wherein said shape detector produces a pulse when said predetermined sequence is detected is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56 of Hebbalalu et al).

In considering claim 19, Hebbalalu et al discloses all claimed subject matter, note 1) the claimed a shape detector for processing samples of an input signal having a series of synchronization pulses and a plurality of non-synchronization pluses to determine whether such samples have a predetermined sequence; said predetermined sequence being a first, non-time varying portion, followed by a first, time-varying portion, followed by a second, non-time varying portion, followed by a second, time varying portion followed by a third, non-time varying portion, one of the first and second, time varying portion having a positive slope and the other one of the first and second, time varying portion having a negative slope, said shape detector producing a shape detection pulse each time said predetermined sequence is detected is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph

illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), 2) the claimed an evaluator responsive to the produced shape pulse detection pulses for determining whether such shape detection pulses are produced at a predetermined rate expected for the series of synchronization pulses is met by the digital circuit 230 which includes the pulse type detection circuit 620 receives the output of operational amplifier 250 and determines whether a valid pulse is present (Fig. 6, col. 5, line 58 to col. 7, line 12).

However, Hebbalalu et al explicitly do not disclose the newly added limitation wherein the slope of the time varying portions are determined by comparing said input signal to a specified criterion based in part of the various slop requirements for the time varying portions.

Hulvey teaches that the falling edge detector 86 essentially forms a circuit with looks for a point in the digitized video signal 14 where the cumulative drop in the three samples is greater than or equal to eight (8) and the last value was less than or equal to two (2), when this condition occurs, the falling edge of the digitized horizontal sync pulse 16 has been detected, the outputs from the binary weighted comparators 102 and 106 are each applied to an AND gate 108, if both inputs to the AND gate to high indicating a flat portion followed by a steep slope (i.e. falling edge), and the AND gate 108 outputs a high timing pulse identified as the external horizontal sync pulse 30 (Figs. 2A and 2B, col. 5, line 35 to col. 7, line 32).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the slope determination as taught by Hulvey into Hebbalalu et al's system in order to accurately detecting and processing horizontal synchronization pulse in the analog video signal.

In considering claim 20, Hebbalalu et al discloses all claimed subject matter, note 1) the claimed a shape detector for processing samples of an input signal having a series of synchronization pulses and a plurality of non-synchronization pulses, each one of said synchronization pulses preceding a segment of the input signal having non-synchronization pulses, to determined whether such samples have a predetermined; said predetermined sequence being a first, non-time varying portion, followed by a first, time-varying portion, followed by a second, non-time varying portion, followed by a second, time varying portion followed by a third, non-time varying portion, one of the first and second, time varying portion having a positive slope and the other one of the first and second, time varying portion having a negative slope, said shape detector producing a shape detection pulse and an associated value for the second, non-time varying portion each time said predetermined sequence is detected is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), 2) the claimed an evaluator responsive to the produced shape detection pulses and said associated values of said second, non-time varying

portions for determining whether one of said associated values of said produced second, non-time varying portions is substantially higher, lower, or the same as a reference value derived from a previous segment of the input signal is met by the biasing circuit 220 which operates to bias the composite video signal received on line 101 to a higher or lower level as determined by digital circuit 230 and the D.C. voltage level can be used for such biasing (Figs. 2, 4 and 6, col. 4, line 24 to col. 5, line 56 and col. 6, line 31 col. 7, line 12).

However, Hebbalalu et al explicitly do not disclose the newly added limitation wherein the slope of the time varying portions are determined by comparing said input signal to a specified criterion based in part of the various slop requirements for the time varying portions.

Hulvey teaches that the falling edge detector 86 essentially forms a circuit with looks for a point in the digitized video signal 14 where the cumulative drop in the three samples is greater than or equal to eight (8) and the last value was less than or equal to two (2), when this condition occurs, the falling edge of the digitized horizontal sync pulse 16 has been detected, the outputs from the binary weighted comparators 102 and 106 are each applied to an AND gate 108, if both inputs to the AND gate to high indicating a flat portion followed by a steep slope (i.e. falling edge), and the AND gate 108 outputs a high timing pulse identified as the external horizontal sync pulse 30 (Figs. 2A and 2B, col. 5, line 35 to col. 7, line 32).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the slope determination as taught by Hulvey into

Hebbalalu et al's system in order to accurately detecting and processing horizontal synchronization pulse in the analog video signal.

In considering claim 23, Hebbalalu et al discloses all claimed subject matter, note 1) the claimed determining, time varying properties of an input signal having the synchronization pulse is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), 2) the claimed comparing the determined, time varying properties with time varying properties expected of the synchronization pulse, and producing, based on the comparison, an output signal indicative of the detection of the synchronization pulse is met by the digital circuit 230 which includes the pulse type detection circuit 620 receives the output of operational amplifier 250 and determines whether a valid pulse is present (Fig. 6, col. 5, line 58 to col. 7, line 12).

However, Hebbalalu et al explicitly do not disclose the newly added limitation the determining time-varying slopes of an input video signal.

Hulvey teaches that the falling edge detector 86 essentially forms a circuit with looks for a point in the digitized video signal 14 where the cumulative drop in the three samples is greater than or equal to eight (8) and the last value was less than or equal to two (2), when this condition occurs, the falling edge of the digitized horizontal sync pulse 16 has been detected, the outputs from the binary weighted comparators 102 and

106 are each applied to an AND gate 108, if both inputs to the AND gate to high indicating a flat portion followed by a steep slope (i.e. falling edge), and the AND gate 108 outputs a high timing pulse identified as the external horizontal sync pulse 30 (Figs. 2A and 2B, col. 5, line 35 to col. 7, line 32).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the slope determination as taught by Hulvey into Hebbalalu et al's system in order to accurately detecting and processing horizontal synchronization pulse in the analog video signal.

Claim 24 is rejected for the same reason as discussed in claim 23.

Claim 25 is rejected for the same reason as discussed in claim 23.

Claim 27 is rejected for the same reason as discussed in claim 13.

7. Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebbalalu et al (US Patent No. 6,130,719) in view of Hulvey (US Patent No. 5,844,622), and further in view of Narusawa (US Patent No. 4,792,852).

In considering claim 21, the combination of Hebbalalu et al and Hulvey discloses all the features of the instant invention as discussed in claim 20 above except for providing the claimed wherein said evaluator includes a time window responsive to the produced shape detection pulses for determining whether said shape detection pulses are produced at a predetermined rate expected for the series of synchronization pulses. Narusawa teaches vertical synchronizing signal detection circuit having a time window responsive to the produced pulses for determining whether such shape detection pulses are produced at a predetermined rate expected for the series of synchronization pulses

(Fig. 1, a window establishing circuit 14, col. 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the 455 counter 16, the window establishing circuit 14, and a horizontal synchronizing signal compensation circuit 18 of Narusawa into the combination of Hebbalalu et al and Hulvey's system in order to accuracy detecting the horizontal synchronizing signal (see col. 1, line 63 to col. 2, line 3 of Narusawa).

In considering claim 26, Hebbalalu et al discloses all the claimed subject matter, note 1) the claimed determining, time varying properties of each of the sequence of input signals to identify one of the portions of such one of the input signals is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), 2) the claimed comparing the determined, time varying properties with time varying properties expected of the one identified one of portions of the synchronization pulse is met by the clamping circuit 120 which recovers the synchronization signals, Fig. 3A is a graph illustrating composite video signal 310 and ideal slicing 311 which would generate composite (including both HSYNC and VSYNC) synchronization signal 312 and the desired composite synchronization signal is represented as target signal 319 (Figs. 2-5, col. 4, line 9 to col. 5, line 56), and 3) the claimed producing, based on the comparison, output signals indicative of the detection of the synchronization pulses of the sequence of input signals is met by the digital circuit

230 which includes the pulse type detection circuit 620 receives the output of operational amplifier 250 and determines whether a valid pulse is present (Fig. 6, col. 5, line 58 to col. 7, line 12). Hebbalalu et al explicitly does not disclose: 1) the determining time-varying slopes of an input video signal, and 2) the claimed comparing rate of production of the output pulses with the predetermined rate of the input signals.

1) Hulvey teaches that the falling edge detector 86 essentially forms a circuit with looks for a point in the digitized video signal 14 where the cumulative drop in the three samples is greater than or equal to eight (8) and the last value was less than or equal to two (2), when this condition occurs, the falling edge of the digitized horizontal sync pulse 16 has been detected, the outputs from the binary weighted comparators 102 and 106 are each applied to an AND gate 108, if both inputs to the AND gate to high indicating a flat portion followed by a steep slope (i.e. falling edge), and the AND gate 108 outputs a high timing pulse identified as the external horizontal sync pulse 30 (Figs. 2A and 2B, col. 5, line 35 to col. 7, line 32).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the slope determination as taught by Hulvey into Hebbalalu et al's system in order to accurately detecting and processing horizontal synchronization pulse in the analog video signal.

2) Narusawa teaches vertical synchronizing signal detection circuit having a 455 counter 16, a window establishing circuit 14, and a horizontal synchronizing signal compensation circuit 18 for comparing rate of production of the output pulses with the predetermined rate of the input signals (col. 3, lines 18-36 of Narusawa).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the 455 counter 16, the window establishing circuit 14, and a horizontal synchronizing signal compensation circuit 18 of Narusawa into Hebbalalu et al's system in order to accuracy detecting the horizontal synchronizing signal (see col. 1, line 63 to col. 2, line 3 of Narusawa).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (703) 305-0090. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT
March 18, 2005

TRANG TRAN
PATENT EXAMINER